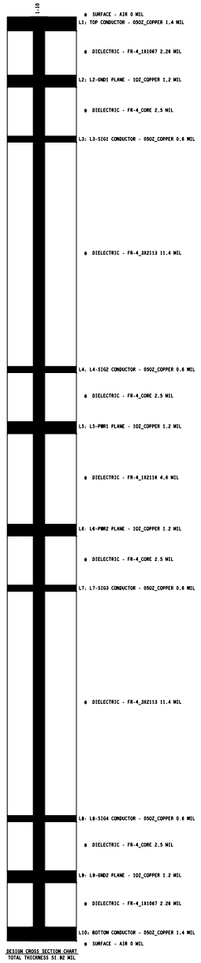
3 STACKUP



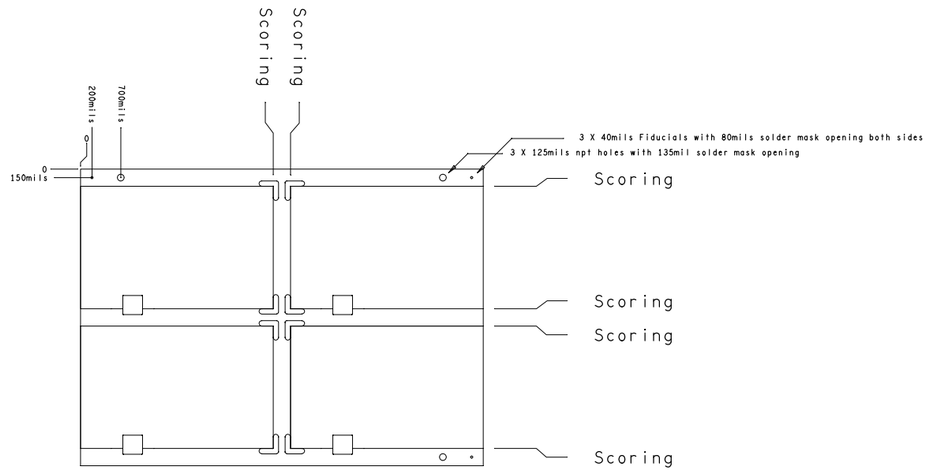
LINE WIDTH IMPEDANCE CHART FOR REFERENCE
Impedances shown are not used on every layer.

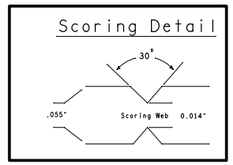
LAYER	SINGLE ENDED LINE WIDTH	DIFF LINE WIDTH	DIFF LINE SPACE	SINGLE	DIFF
L1,L10	N/A	3.2 MILS	8.8 MILS	N/A	100 OHMS
L1,L10	N/A	3.3 MILS	4.7 MILS	N/A	90 OHMS
~~L1~~	~~N/A~~	~~3.7 MILS~~	~~4.3 MILS~~	~~N/A~~	~~85 OHMS~~
~~L1~~	~~N/A~~	~~4.4 MILS~~	~~3.6 MILS~~	~~N/A~~	~~76 OHMS~~
L1,L10	3.5 MILS	N/A	N/A	50 OHMS	N/A
L3,L4 L7,L8	N/A	3 MILS	7 MILS	N/A	100 OHMS
L3,L4 L7,L8	3.25 MILS	N/A	N/A	50 OHMS	N/A
L3,L4	N/A	3.4 MILS	4.6 MILS	N/A	90 OHMS
L3,L4 L7,L8	N/A	3.7 MILS	4.3 MILS	N/A	85 OHMS
~~L3,L4 L7,L8~~	~~N/A~~	~~4.4 MILS~~	~~3.6 MILS~~	~~N/A~~	~~76 OHMS~~
~~L3,L4 L7,L8~~	~~N/A~~	~~3.6 MILS~~	~~4.4 MILS~~	~~N/A~~	~~86 OHMS~~
~~L3,L4 L7,L8~~	~~5.5 MILS~~	~~N/A~~	~~N/A~~	~~39 OHMS~~	~~N/A~~
~~L3,L4 L7,L8~~	~~6.3 MILS~~	~~N/A~~	~~N/A~~	~~36 OHMS~~	~~N/A~~
~~L10~~	~~N/A~~	~~4.4 MILS~~	~~3.6 MILS~~	~~N/A~~	~~76 OHMS~~
L10	N/A	3.7 MILS	4.3 MILS	N/A	85 OHMS
~~L7,L8~~	~~N/A~~	~~3.4 MILS~~	~~4.6 MILS~~	~~N/A~~	~~90 OHMS~~

CROSSED IMPEDANCE CALL OUTS DO NOT EXIST IN PROVIDED DATA. IGNORE THEM.

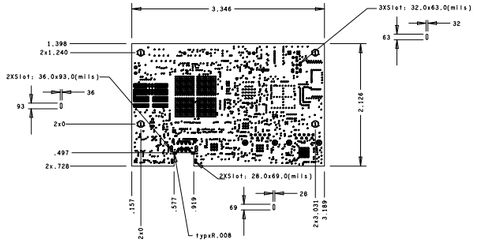
DRILL CHART: TOP to BOTTOM
ALL UNITS ARE IN MILS

FIGURE	SIZE	TOLERANCE	PLATED	QTY
✶	6.0	+0.0/-6.0	PLATED	201
•	8.0	+0.0/-8.0	PLATED	1559
✶	10.0	+0.0/-10.0	PLATED	65
✶	12.0	+0.0/-12.0	PLATED	41
✶	16.0	+0.0/-16.0	PLATED	18
✶	22.0	+1.0/-1.0	PLATED	20
✶	28.0	+3.0/-3.0	PLATED	18
●	40.0	+3.0/-3.0	PLATED	2
⓫	91.0	+2.0/-2.0	PLATED	2
⓭	111.0	+2.0/-2.0	PLATED	4
■	20.0	+2.0/-2.0	NON-PLATED	2
■	32.0	+2.0/-2.0	NON-PLATED	1
■	40.0	+2.0/-2.0	NON-PLATED	2
■	47.0	+2.0/-2.0	NON-PLATED	4
■	48.0	+2.0/-2.0	NON-PLATED	1
■	52.0	+2.0/-2.0	NON-PLATED	2
▮	63.0x32.0	+3.0/-3.0	PLATED	3
▮	69.0x28.0	+3.0/-3.0	PLATED	2
▮	93.0x36.0	+3.0/-3.0	PLATED	2





Array size X = 6.992" Y = 5.152"
Board to board distance 300mil
Rail area 300mils



NOTES:

1. FABRICATE TO IPC-6012 CLASS 2,CURRENT REVISION.
2. BOARD SHALL MEET THE INSPECTION CRITERIA OF IPC-A-600,CLASS 2,CURRENT REVISION.
3. MATERIAL: ISOLA 370 HR.
4. WEIGHT OF ALL COPPER LAYERS SHALL NOT BE LESS 0.5 OZ. PER SQUARE FOOT.
5. IMPEDANCE TOLERANCE +/-10% FOR ALL LAYERS.
6. APPLY SOLDER MASK OVER BARE COPPER(SMBOC) IAW IPC-SM-840,BOTH SIDES,USING LPI,COLOR BLACK.
7. FINISH: ENIG
8. SILKSCREEN TOP SIDE/BOTH SIDES WITH NON-CONDUCTIVE EPOXY BASED INK. COLOR SHALL BE WHITE. DISTORTION OF SILKSCREEN IS ACCEPTABLE OVER TRACES. EPOXY INK ON PLATED LANDS IS NOT ACCEPTABLE.
9. VENDOR LOGO, FLAMMABILTY AND DATE CODE TO BE MARKED FAR SIDE SILK SCREEN.
10. 100% ELECTRICAL TEST REQUIRED FOR CONTINUITY. BOARD SHALL HAVE A UL RATING OF 94V-0. UL SYMBOL AND RATING SHALL BE MARKED FARSIDE IN COPPER.
11. REMOVE ALL UNUSED PADS FROM INTERNAL LAYERS.
12. SOLDER MASK REGISTRATION TO BE WITHIN DIAMETRICAL TRUE POSITION OF + / - 0.002 WITH APPLICABLE HOLE / PAD.
13. SOLDER MASK REQUIREMENTS FOR VIAS:
    a) VIA DRILLS TENTED(COVERED)FROM TOP SIDE AND ENCROACHED WITH SOLDER MASK RELIEF OF DRILL PLUS 6MIL FROM BOTTOM.
    b) PLUG TENTED VIAS.
14. 274X GERBERS/ODB++ USED FOR FAB MUST BE VERIFIED AGAINST THE PROVIDED IPC356 NETLIST.
15. USE ARTMASTER # AES_ULTRA96-G_REV1
16. THIEVING: DO NOT ADD COPPER THIEVING ON TOP LAYER IN THE FBGA AREA. THIEVING PATTERN IS TO BE 30 MILS SQUARE PADS, 50 MILS SPACING. THIEVING ALLOWED ON INTERNAL LAYERS TO ACHIEVE BALANCED COPPER DENSITY, MAINTAIN 150 MIL CLEAREANCE TO COPPER FEATURES. DO NOT ADD THIEVNG UNDER SILKSCREEN TEXT IF POSIBLE
17. BUILD BOARDS ON A PANEL IN A BEST FIT ARRAY, 250 MIL SPACING MINIMUM, MOUSE BITS OK.
18. ALL VIA-IN-PADS TO BE COMPLETELY FILLED, PLANARIZED, SMOOTH AND PLATED OVER ON SURFACE. USE SanEi NON-CONDUCTIVE EPOXY OR EQUIVALENT FILL MATERIALS MINIMUM OF .0007 TO BE PLATED ON SURFACE. VIA-IN-PAD MUST INCLUDE WRAP REQUIREMENTS PER IPC 6012B.
19. PCB VENDOR MAY ADD TEARDROPS AS REQUIRED TO ALL SIGNAL LAYERS. DRC CHECKS MUST BE RUN AFTER IMPLEMENTATION.
20. FOLLOWING ARE INTENTIONAL SHORTS.
    1- VCC_1V2 Shorted to BUCK_FB5
    2- VCC_3V3 Shorted to BUCK_FB4
    3- GND Shorted to FBOUT2_N SNS1, SNS6, SNS2
    4- VCC_PSAUX Shorted to FBOUT6
    5- VCCO_PSDDR Shorted to BUCK_FB3
    6- MGTRAVCC Shorted to 5352N440
    7- VCC_PSINTLP Shorted to FBOUT2_P

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
A	PROTOTYPE	05-11-16	
B		11-29-16	
C		06-14-17	
D		07-19-17	

UNLESS OTHERWISE SPECIFIED	SIGNATURES		DATE
DIMENSIONS ARE IN INCHES	DRAWN	AVNET DESIGN	03-15-18
TOLERANCES ON;	CHECKED		
2 PL DECIMALS +/- .010	ENGRG	B. FORSSE	06-14-17
3 PL DECIMALS +/- .005	ISSUED		
ANGLES +			
FRACTIONS +			

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PCB, ROHS COMPLIANT
AES-ULTRA96-G
www.ultra96.org
FABRICATION / DRILL DRAWING

SIZE	DWG NO	REV
D	PWB-USDEV1	1

SCALE NONE SHEET 1 OF 1